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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/529,170	03/24/2005	Martin J Edwards	GB02 0173 US	4332

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EXAMINER	
JEANGLAUDE, JEAN BRUNER	
ART UNIT	**PAPER NUMBER**
2819	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/529,170	EDWARDS ET AL.	
	Examiner	Art Unit	
	Jean B. Jeanglaude	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3-24-05*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Information Disclosure Statement

The information Disclosure Statement (IDS) is not considered because the numbers written in the IDS are incorrect.

Continuing Data

It is suggested to incorporated the continuing data in the first page of the invention as the first paragraph.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 – 4, 11, 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujino (USPGPUB 2002/0080131).

3. Regarding claim 1, Fujino discloses an active matrix array device (figs. 13, 16, 17, 18, 19) comprising an array of individually addressable matrix elements and driver circuitry (902, fig. 13) for providing address signals to the matrix elements (abstract; paragraphs 0001, 0014, 0022), the driver circuitry (902, fig. 13) including digital to

analogue converter circuitry (1309, fig. 13) for providing a first number of outputs for application in parallel to a corresponding first number of matrix elements, wherein the driver circuitry is arranged alongside one edge of the array of matrix elements, and comprises: a multiple voltage level generator circuit providing a plurality of analogue voltage levels (1309, fig. 13; 1309, fig. 16) for addressing the matrix elements, the plurality of levels being provided on outputs distributed substantially along the length of the one edge (figs. 13, 16) ; a group of switches (note the switches in fig. 18) associated with, and located at, each output of the voltage level generator circuit (figs. 13, 16, 17, 18); and an output bus (the output of the DAC 1306) arranged alongside the one edge and having the first number of lines, the group of switches selectively coupling the associated voltage level generator circuit output to each line of the output bus (figs. 13, 16, 17, 18, 19).

4. Regarding claim 2, Fujino discloses a device (figs. 13, 16, 17, 18, 19), wherein the multiple voltage level generator circuit (1309, fig. 16) comprises a resistor string extending alongside the length of the one edge (R_0,..., R_7).

5. Regarding claim 3, Fujino discloses a device (figs. 13, 16, 17, 18, 19), wherein each group (the switching elements in fig. 18) of switches comprises a switch associated with each output bus line.

6. Regarding claim 11, Fujino discloses a device (figs. 13, 16 – 19) discloses a device comprising an active matrix liquid crystal display (title).

7. Regarding claim 12, Fujino discloses a device (figs. 13, 16 – 19), wherein the driver circuitry (902) is integrated onto the same substrate as the array of matrix elements (fig. 13).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 4 - 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujino in view of Ichikawa et al. (US Patent Number 5,028,916).

10. Regarding claims 4 – 10, Fujino discloses all the limitations as discussed above the except the device wherein the switches of each group are controlled by a corresponding bit of digital words based on the digital inputs to the digital to analogue converter circuitry (claim 4) ; the device (figs. 13, 16 – 19) a device wherein the digital words comprise the expansion of n-bit digital inputs to the digital to analogue converter circuitry into 2.sup.n bit words having a single non-zero bit (claim 5); the device further comprising a multiplexer circuit for switching the first number (X) of outputs to a selected first number of matrix element (claim 6); the device wherein the array of matrix elements are arranged in rows and columns, and the driver circuitry is arranged alongside a column edge of the array, and wherein the multiplexer circuit switches the first number of outputs to a selected subset of the columns (claim 7); the device wherein the multiplexer circuit comprises the output bus and switching elements which

connect to the output bus and to each column (claim 8); the device comprising decoder circuitry for converting n-bit digital inputs to the digital to analogue converter circuitry into 2.sup.n bit words having a single non-zero bit (claim 9); the device wherein the decoder circuitry is distributed along the length of the one edge and receives the first number of n-bit digital inputs (Data1-DataX), and generates the first number of 2.sup.n bit digital outputs, with corresponding bits of each of the first number of 2.sup.n bit digital outputs spatially grouped together (claim 10). However, Ichikawa et al., in a related field, discloses a device wherein the switches of each group are controlled by a corresponding bit of digital words based on the digital inputs to the digital to analogue converter circuitry (figs.1, 7, 10A – 10C, 12, 16; abstract, col. 2, lines 7 - 27) ; the device wherein the digital words comprise the expansion of n-bit digital inputs to the digital to analogue converter circuitry into 2.sup.n bit words having a single non-zero bit (figs.1, 7, 10A – 10C, 12, 16; abstract, col. 2, lines 7 - 27); the device further comprising a multiplexer circuit for switching the first number (X) of outputs to a selected first number of matrix element (figs.1, 7, 10A – 10C, 12, 16; abstract, col. 2, lines 7 - 27); the device wherein the array of matrix elements are arranged in rows and columns, and the driver circuitry is arranged alongside a column edge of the array, and wherein the multiplexer circuit switches the first number of outputs to a selected subset of the columns (figs.1, 7, 10A – 10C, 12, 16; abstract, col. 2, lines 7 - 27); the device wherein the multiplexer circuit comprises the output bus and switching elements which connect to the output bus and to each column (figs.1, 7, 10A – 10C, 12, 16; abstract, col. 2, lines 7 – 27; col. 10, lines 22 - 35); the device comprising decoder circuitry for converting n-

bit digital inputs to the digital to analogue converter circuitry into 2.sup.n bit words having a single non-zero bit (figs.1, 7, 10A – 10C, 12, 16; abstract, col. 2, lines 7 – 27; col. 10, lines 22 - 35); the device wherein the decoder circuitry is distributed along the length of the one edge and receives the first number of n-bit digital inputs (Data1-DataX), and generates the first number of 2.sup.n bit digital outputs, with corresponding bits of each of the first number of 2.sup.n bit digital outputs spatially grouped together (figs.1, 7, 10A – 10C, 12, 16; abstract, col. 2, lines 7 – 27; col. 10, lines 22 - 35). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Fujino's system with that of Ichikawa et al.'s system in order to provide a display of a thin that performs a fast and efficient display drive operation with a simplified circuit configuration.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. (See PTO-892).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B. Jeanglaude whose telephone number is 571-272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jean Bruner Jeanglaude
Primary Examiner
February 8, 2007